CLAIMS

[0073] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A photodiode for use in an imaging device, said photodiode comprising:

a first layer of a first conductivity type formed below a surface of a substrate and laterally displaced from an electrically active portion of a gate of a transistor, said first layer having a thickness of about 100 Angstroms to about 500 Angstroms; and

a charge collection region of a second conductivity type formed below said first layer for accumulating photo-generated charge, said charge collection region being adjacent said transistor gate.

2. The photodiode of claim 1, wherein said first layer has a thickness of about 100 Angstroms to about 300 Angstroms.

3. The photodiode of claim 2, wherein said first layer has a thickness of about 250 Angstroms.

4. The photodiode of claim 1, wherein said first layer is doped with a p-type dopant at a dopant concentration of from about 5×10^{17} atoms per cm^3 to about 1×10^{19} atoms per cm^3.

5. The photodiode of claim 4, wherein said first layer is doped with a p-type dopant at a dopant concentration of about 1 x 10^{18} atoms per cm^3 to about 5 x 10^{18} atoms per cm^3.

6. The photodiode of claim 1, wherein said first layer is a pinned layer.

7. The photodiode of claim 1, wherein said first layer is in contact with an isolation region formed within said substrate.

8. The photodiode of claim 1, wherein said gate is a transfer transistor gate for transferring charge accumulated in said charge collection region to a doped region of said second conductivity type.

9. The photodiode of claim 1, wherein said first conductivity type is p-type and said second conductivity type is n-type.

10. The photodiode of claim 1, wherein said charge collection region is doped with an n-type dopant at a dopant concentration of about 3 x 10^{15} to about 1 x 10^{18} atoms per cm^3.

11. The photodiode of claim 1, wherein said photodiode is a p-n-p photodiode.

12. The photodiode of claim 1, wherein said transistor is part of one of a 3T, 4T, 5T, 6T or 7T pixel sensor cell.

13. The photodiode of claim 1, wherein said transistor is part of a CMOS imager.

14. The photodiode of claim 1, wherein said transistor is part of a CCD imager.

15. An image pixel comprising:

a gate structure of a transistor formed over a semiconductor substrate; and

a photodiode adjacent said gate, said photodiode comprising a surface layer of a first conductivity type located below a surface of said semiconductor substrate and a doped region of a second conductivity type located below said surface layer, said surface layer having a thickness of about 100 Angstroms to about 500 Angstroms and a dopant concentration of about 5×10^{17} atoms per cm^3 to about 1×10^{19} atoms per cm^3.

16. The image pixel of claim 15, wherein said surface layer has a thickness of about 100 Angstroms to about 300 Angstroms.

17. The image pixel of claim 16, wherein said surface layer has a thickness of about 250 Angstroms.

18. The image pixel of claim 15, wherein said surface layer has a dopant concentration of about 1×10^{18} atoms per cm^3 to about 5×10^{18} atoms per cm^3.

19. The image pixel of claim 15, wherein said surface layer is adjacent and in contact with an isolation region formed within said semiconductor substrate.

20. The image pixel of claim 15, wherein said first conductivity type is p-type and said second conductivity type is n-type.

21. The image pixel of claim 15, wherein said surface layer is doped with boron or indium.

22. The image pixel of claim 15, wherein said surface layer is doped with arsenic or antimony at a dopant concentration of about 3×10^{15} atoms per cm^3 to about 1×10^{18} atoms per cm^3.

23. The image pixel of claim 15, wherein said photodiode is a p-n-p photodiode.

24. The image pixel of claim 15, wherein said transistor is part of one of a 3T, 4T, 5T, 6T or 7T pixel sensor cell.

25. The image pixel of claim 15, wherein said transistor is part of a CMOS imager.

26. The image pixel of claim 15, wherein said transistor is part of a CCD imager.

27. A photodiode of an image sensor comprising:

a surface layer of a first conductivity type adjacent a gate of a transistor, said gate being formed over a silicon substrate, said surface layer being

located below a surface of said silicon substrate to a depth of about 100 Angstroms to about 500 Angstroms; and

a doped region of a second conductivity type located below said surface layer.

28. The photodiode of claim 27, wherein said surface layer is located below said surface of said silicon substrate to a depth of about 100 Angstroms to about 300 Angstroms.

29. The photodiode of claim 28, wherein said surface layer is located below said surface of said silicon substrate to a depth of about 250 Angstroms.

30. The photodiode of claim 27, wherein said surface layer is doped with a p-type dopant at a dopant concentration of from about 5×10^{17} atoms per cm^3 to about 1×10^{19} atoms per cm^3.

31. The photodiode of claim 30, wherein said surface layer is doped with a p-type dopant at a dopant concentration of about 1×10^{18} atoms per cm^3 to about 5×10^{18} atoms per cm^3.

32. The photodiode of claim 30, wherein said p-type dopant is boron or indium.

33. The photodiode of claim 27, wherein said surface layer is adjacent and in contact with an isolation region formed within said silicon substrate.

34. The photodiode of claim 27, wherein said surface layer and said doped region are both located within a doped layer of said first conductivity type.

35. The photodiode of claim 27, wherein said transistor is part of a CMOS imager.

36. The photodiode of claim 27, wherein said transistor is part of a CCD imager.

37. The photodiode of claim 27, wherein said transistor is part of a 4T pixel sensor cell.

38. The photodiode of claim 27, wherein said transistor is part of a 3T pixel sensor cell.

39. An imager system comprising:

(i) a processor; and

(ii) an imaging device coupled to said processor, said imaging device comprising:

a field isolation region formed in a substrate; and

a pixel adjacent said field isolation region, said pixel comprising a p-n-p photodiode adjacent a gate of a transfer transistor, said p-n-p photodiode further comprising a p-type surface layer and an n-type doped region located below said p-type surface layer, said p-type surface layer having a thickness of about 100 Angstroms to about 500 Angstroms.

40. The system of claim 39, wherein said p-type surface layer has a thickness of about 100 Angstroms to about 300 Angstroms.

41. The system of claim 40, wherein said p-type surface layer has a thickness of about 250 Angstroms.

42. The system of claim 39, wherein said surface layer is doped with a p-type dopant at a dopant concentration of from about 5×10^{17} atoms per cm^3 to about 1×10^{19} atoms per cm^3.

43. The system of claim 42, wherein said surface layer is doped with a p-type dopant at a dopant concentration of about 1×10^{18} atoms per cm^3 to about 5×10^{18} atoms per cm^3.

44. The system of claim 39, wherein said p-type surface layer is adjacent and in contact with said field oxide region.

45. The system of claim 39, wherein said p-type surface layer and said n-type doped region are both located within a p-type doped region.

46. The system of claim 39, wherein said pixel is one of a 3T, 4T, 5T, 6T or 7T pixel sensor cell.

47. The system of claim 39, wherein said imaging device is a CMOS imaging device.

48. The system of claim 39, wherein said imaging device is a CCD imaging device.

49. A method of forming a photodiode for a pixel sensor cell, said method comprising:

forming a gate of a transistor over a substrate;

forming a first doped layer of a first conductivity type in said substrate and adjacent said gate, said first doped layer being formed to a thickness of about 100 Angstroms to about 500 Angstroms; and

forming a doped region of a second conductivity type in said substrate and below said first doped layer.

50. The method of claim 49, wherein said first doped layer has a dopant concentration within the range of from about 5×10^{17} atoms per cm^3 to about 1×10^{19} atoms per cm^3.

51. The method of claim 50, wherein said first doped layer has a dopant concentration of about 1×10^{18} atoms per cm^3 to about 5×10^{18} atoms per cm^3.

52. The method of claim 49, wherein said first doped layer is formed to a thickness of about 100 Angstroms to about 300 Angstroms.

53. The method of claim 52, wherein said first doped layer is formed to a thickness of about 250 Angstroms.

54. The method of claim 49, wherein said act of forming said first doped layer further comprises forming an in-situ doped layer of said first conductivity type over a first area of said substrate.

55. The method of claim 54, wherein said act of forming said first doped layer further comprises diffusing ions from said in-situ doped layer into said first area of said substrate.

56. The method of claim 55, wherein said act of diffusing said ions from said in-situ doped layer further comprises annealing said in-situ doped layer at a temperature of about 900°C to about 1100°C.

57. The method of claim 56, wherein said act of annealing said in-situ doped layer is conducted for about 10 seconds to about 20 seconds.

58. The method of claim 56, wherein said act of annealing said in-situ doped layer is conducted at a temperature of about 950°C to about 1000°C for about 10 seconds to about 20 seconds.

59. The method of claim 49, wherein said act of forming said first doped layer further comprises forming an undoped oxide layer over a second area of said substrate.

60. The method of claim 59, wherein said act of forming said first doped layer further comprises implanting ions of said first conductivity type in said undoped oxide layer to form a doped oxide layer.

61. The method of claim 60, wherein said act of forming said first doped layer further comprises diffusing ions from said doped oxide layer into said second area of said substrate to form said first doped layer.

62. The method of claim 61, wherein said act of diffusing said ions from said doped oxide layer further comprises annealing said doped oxide layer at a temperature of about 900°C to about 1100°C.

63. The method of claim 62, wherein said act of annealing said doped oxide layer is conducted for about 10 seconds to about 20 seconds.

64. The method of claim 62, wherein said act of annealing said doped oxide layer is conducted at a temperature of about 950°C to about 1000°C and for about 10 seconds to about 20 seconds.

65. The method of claim 49, wherein said act of forming said first doped layer further comprises conducting a gas source plasma doping in a third area of said substrate.

66. The method of claim 65, wherein said gas source plasma doping is conducted in a B_2H_6 plasma diluted by another gas.

67. The method of claim 66, wherein said another gas is helium.

68. The method of claim 65, wherein said gas source plasma doping is conducted in a BF_2 plasma diluted by another gas.

69. The method of claim 68, wherein said another gas is helium.

70. The method of claim 65, wherein said gas source plasma doping is conducted in an electron cyclotron (ECR) for about 100 seconds.

71. The method of claim 65, wherein said gas source plasma doping is conducted in a radio frequency (RF) plasma source for about 100 seconds.

72. The method of claim 49, wherein said doped region has a dopant concentration within the range of from about 3×10^{15} to about 1×10^{18} atoms per cm^3.

73. The method of claim 49, wherein said first conductivity type is p-type and said second conductivity type is n-type.

74. The method of claim 49, wherein said photodiode is a p-n-p photodiode.

75. The method of claim 49, wherein said pixel sensor cell is one of a 3T, 4T, 5T, 6T or 7T sensor cell.

76. The method of claim 49, wherein said pixel sensor cell is part of a CMOS imager.

77. The method of claim 49, wherein said pixel sensor cell is part of a CCD imager.

78. A method of forming a photodiode, said method comprising:

forming at least one shallow trench isolation region in a silicon substrate;

forming a transistor gate over said silicon substrate and spaced apart from said at least one shallow trench isolation region;

forming an ultra-shallow first doped layer of a first conductivity type below a surface of said silicon substrate and laterally displaced from said transistor gate, said ultra-shallow first doped layer having a dopant concentration within the range of from about 5×10^{17} atoms per cm^3 to about 1×10^{19} atoms per cm^3; and

forming a doped region of a second conductivity type in said silicon substrate and below and in contact with said ultra-shallow first doped layer.

79. The method of claim 78, wherein said first doped layer has a dopant concentration of about 1×10^{18} atoms per cm^3 to about 5×10^{18} atoms per cm^3.

80. The method of claim 78, wherein said doped region has a dopant concentration within the range of from about 3×10^{15} to about 1×10^{18} atoms per cm^3.

81. The method of claim 78, wherein said act of forming said ultra-shallow first doped layer further comprises forming an in-situ doped layer of said first conductivity type over a first area of said substrate.

82. The method of claim 81, wherein said act of forming said ultra-shallow first doped layer further comprises diffusing ions from said in-situ doped layer into said first area of said substrate.

83. The method of claim 82, wherein said act of diffusing said ions from said in-situ doped layer further comprises annealing said in-situ doped layer at a temperature of about 900°C to about 1100°C.

84. The method of claim 83, wherein said act of annealing said in-situ doped layer is conducted for about 10 seconds to about 20 seconds.

85. The method of claim 83, wherein said act of annealing said in-situ doped layer is conducted at a temperature of about 950°C to about 1000°C and for about 10 seconds to about 20 seconds.

86. The method of claim 78, wherein said act of forming said ultra-shallow first doped layer further comprises forming an undoped oxide layer over a second area of said substrate.

87. The method of claim 86, wherein said act of forming said ultra-shallow first doped layer further comprises implanting ions of said first conductivity type in said undoped oxide layer to form a doped oxide layer.

88. The method of claim 87, wherein said act of forming said ultra-shallow first doped layer further comprises diffusing ions from said doped oxide layer into said second area of said substrate to form said first doped layer.

89. The method of claim 88, wherein said act of diffusing said ions from said doped oxide layer further comprises annealing said doped oxide layer at a temperature of about 900°C to about 1100°C.

90. The method of claim 89, wherein said act of annealing said doped oxide layer is conducted for about 10 seconds to about 20 seconds.

91. The method of claim 89, wherein said act of annealing said doped oxide layer is conducted at a temperature of about 950°C to about 1000°C and for about 10 seconds to about 20 seconds.

92. The method of claim 78, wherein said act of forming said ultra-shallow first doped layer further comprises conducting a gas source plasma doping in a third area of said substrate.

93. The method of claim 92, wherein said gas source plasma doping is conducted in a B_2H_6 plasma diluted by another gas.

94. The method of claim 93, wherein said another gas is helium.

95. The method of claim 92, wherein said gas source plasma doping is conducted in a BF_2 plasma diluted by another gas.

96. The method of claim 95, wherein said another gas is helium.

97. The method of claim 92, wherein said gas source plasma doping is conducted in an electron cyclotron (ECR) for about 100 seconds.

98. The method of claim 92, wherein said gas source plasma doping is conducted in a radio frequency (RF) plasma source for about 100 seconds.

99. The method of claim 78, wherein said transistor gate is part of one of a 3T, 4T, 5T, 6T or 7T pixel sensor cell.

100. The method of claim 78, wherein said transistor gate is part of a CMOS imager.

101. The method of claim 78, wherein said transistor gate is part of a CCD imager.

102. A method of forming a photodiode, said method comprising:

forming at least one field oxide region in a substrate;

forming a transistor gate over said substrate and spaced apart from said at least one field oxide region;

conducting a first dopant implantation to form a doped region of a second conductivity type in said substrate and laterally displaced from said transistor gate;

forming an in-situ doped layer of said first conductivity type over a first area of said substrate, said first area being located between an electrically active area of said transistor gate and said field oxide region; and

diffusing ions from said in-situ doped layer into said first area of said substrate to form an ultra-shallow doped layer in said substrate, said ultra-shallow doped layer being in contact with said doped region of said second conductivity type.

103. The method of claim 102, wherein said act of diffusing said ions from said in-situ doped layer further comprises annealing said in-situ doped layer at a temperature of about 900°C to about 1100°C.

104. The method of claim 103, wherein said act of annealing said in-situ doped layer is conducted for about 10 seconds to about 20 seconds.

105. The method of claim 103, wherein said act of annealing said in-situ doped layer is conducted at a temperature of about 950°C to about 1000°C and for about 10 seconds to about 20 seconds.

106. The method of claim 102, wherein said ultra-shallow doped layer has a dopant concentration within the range of from about 5×10^{17} atoms per cm^3 to about 1×10^{19} atoms per cm^3.

107. The method of claim 106, wherein said ultra-shallow doped layer has a dopant concentration of about 1×10^{18} atoms per cm^3 to about 5×10^{18} atoms per cm^3.

108. The method of claim 102, wherein said doped region has a dopant concentration within the range of from about 3×10^{15} to about 1×10^{18} atoms per cm^3.

109. A method of forming a photodiode, said method comprising:

forming at least one field oxide region in a substrate;

forming a transistor gate of a pixel sensor cell over said substrate and spaced apart from said at least one field oxide region;

conducting a first dopant implantation to form a doped region of a second conductivity type in said substrate, said doped region being laterally displaced from said transistor gate;

forming an undoped oxide layer over a first area of said substrate, said first area being located between an electrically active area of said transistor gate and said field oxide region;

implanting ions of said first conductivity type in said undoped oxide layer to form a doped oxide layer; and

diffusing ions from said doped oxide layer into said first area of said substrate to form an ultra-shallow doped layer in said substrate, said ultra-shallow doped layer being in contact with said doped region of said second conductivity type and being laterally displaced from said transistor gate.

110. The method of claim 109, wherein said act of diffusing said ions from said doped oxide layer further comprises annealing said in situ doped layer at a temperature of about 900°C to about 1100°C.

111. The method of claim 110, wherein said act of annealing said doped oxide layer is conducted for about 10 seconds to about 20 seconds.

112. The method of claim 110, wherein said act of annealing said doped oxide layer is conducted at a temperature of about 950°C to about 1000°C and for about 10 seconds to about 20 seconds.

113. The method of claim 109, wherein said ultra-shallow doped layer has a dopant concentration within the range of from about 5×10^{17} atoms per cm^3 to about 1×10^{19} atoms per cm^3.

114. The method of claim 113, wherein said ultra-shallow doped layer has a dopant concentration of about 1×10^{18} atoms per cm^3 to about 5×10^{18} atoms per cm^3.

115. The method of claim 109, wherein said doped region has a dopant concentration within the range of from about 3×10^{15} to about 1×10^{18} atoms per cm^3.

116. The method of claim 109, wherein said pixel sensor cell is one of a 3T, 4T, 5T, 6T or 7T pixel cell.

117. The method of claim 109, wherein said pixel sensor cell is part of a CMOS imager.

118. The method of claim 109, wherein said pixel sensor cell is part of a CCD imager.

119. A method of forming a photodiode, said method comprising:

forming at least one field oxide region in a substrate;

forming a transistor gate over said substrate and spaced apart from said at least one field oxide region;

conducting a first dopant implantation to form a doped region of a second conductivity type in said substrate; and

conducting a plasma doping over a first area of said substrate to form an ultra-shallow doped layer in said substrate, said first area being located between an electrically active area of said transistor gate and said field oxide region, said ultra-shallow doped layer being in contact with said doped region of said second conductivity type.

120. The method of claim 119, wherein said plasma doping is a gas source plasma doping.

121. The method of claim 120, wherein said gas source plasma doping is conducted in a B_2H_6 plasma diluted by another gas.

122. The method of claim 121, wherein said another gas is helium.

123. The method of claim 120, wherein said gas source plasma doping is conducted in a BF_2 plasma diluted by another gas.

124. The method of claim 123, wherein said another gas is helium.

125. The method of claim 120, wherein said gas source plasma doping is conducted in an electron cyclotron (ECR) for about 100 seconds.

126. The method of claim 120, wherein said gas source plasma doping is conducted in a radio frequency (RF) plasma source for about 100 seconds.

127. The method of claim 119, wherein said ultra-shallow doped layer has a dopant concentration within the range of from about 5×10^{17} atoms per cm^3 to about 1×10^{19} atoms per cm^3.

128. The method of claim 127, wherein said ultra-shallow doped layer has a dopant concentration of about 1×10^{18} atoms per cm^3 to about 5×10^{18} atoms per cm^3.

129. The method of claim 119, wherein said doped region has a dopant concentration within the range of from about 3×10^{15} to about 1×10^{18} atoms per cm^3.

130. The method of claim 119, wherein said photodiode is part of a CMOS imager.

131. The method of claim 119, wherein said photodiode is part of a CCD imager.